REMARKS

Claims 1-33 remain pending in the application. Claims 3, 10, 14, and 26 have been amended. Applicants submits the amendments do not raise any new issues of patentability.

35 U.S.C. § 112 Rejection and Objection to the Claims:

Claim 26 was rejected under 35 U.S.C. § 112. Applicant submits that the current amendment to claim 26 overcomes this rejection.

Claims 3 and 14 were objected to for various informalities. Applicant submits that the amendments to these claims overcome the objections.

35 U.S.C. § 103 Rejections:

Claims 1, 3, 5, 8, 10, 22, 24 and 25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara, U.S. Patent 6,629,281, in view of Kim, U.S. Patent 5,938,784, in view of Pouya, U.S. Patent 6701476, and in further view of Udawatta, U.S. Patent 6,738,939. Claims 2, 9, and 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara in view of Kim and Pouya and in further view of Udawatta and Bardell, U.S. Patent 4,959,832. Claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara in view of Kim, Pouya, and Udawatta, and in further view of Simpson, U.S. Patent 5,260,950, Wong, U.S. Patent 6,636,997, and Bogholtz, U.S. Patent 5,357,523. Claims 7, 11, and 28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara in view of Kim, Pouya, and Udawatta, and in further view of Rajski, U.S. Patent 5,991,909. Claims 6, 12, 14, 16, 17, 18, and 27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara in view of Kim, Pouya, and Udawatta, and in further view of Motika, U.S. Patent 5,982,189. Claim 13 was rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara in view of Kim, Pouya, and Udawatta, and in further view of Motika and Bardell. Claim 15 was rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara in view of Kim, Pouya, and Udawatta, and in further view of Motika, Simpson, Wong, and Bogholtz. Claim 19

was rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara in view of Kim, Pouya, and Udawatta, and in further view of Motika and Kim, U.S. Patent 6,148,426 ('Kim 2'). Claim 20 was rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara in view of Kim, Pouya, and Udawatta, and in further view of Motika and Au, U.S. Patent 6,681,359. Claim 21 was rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara in view of Kim, Pouya, and Udawatta, and in further view of Motika and Rajski. Claim 26 was rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara in view of Kim, Pouya, and Udawatta, and in further view of Wong and Bogholtz. Claims 29, 31, 32, and 33 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Au in view of Rajski and in further view of Kim, Pouya, and Udawatta. Claim 30 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Au in view of Rajski, Kim, and Bardell. Applicant respectfully traverses these rejections.

The cited references, taken singly or in combination, do not teach or suggest all of the elements of the independent claims. McNamara describes a method and apparatus, contained within an integrated circuit, for isolating failure by precisely controlling the number of clocks applied during built-in self-test (BIST). A programmable clock counter, on the integrated circuit, stores a specified number of clock cycles and sends a signal to stop a BIST engine once the specified number of clock cycles have been generated. The intermediate results can then be mapped bit by bit in order to isolate the cause of failure.

Kim teaches a built-in self test (BIST) circuit using a linear feedback shift register (LFSR) and a multiple input signature register (MISR) requiring reduced circuitry exclusive of the number of inputs and outputs of the circuit to be tested. The BIST circuit is built in a prescribed circuit having a memory to test a target circuit in the prescribed circuit. The BIST circuit includes an LFSR, including a first logic section which is composed of a plurality of XOR gates and selection sections, and a first memory which is a part of the memory, for performing a primitive polynomial, an MISR, including a second logic section which is composed of a plurality of XOR gates and selection

sections, and a second memory which is a part of the memory, for performing the primitive polynomial, and a BIST control section for controlling data input/output between the first and second memories and the target circuit and providing selection signals for controlling the selection sections in the first and second logic sections, the BIST control section controlling the target circuit and comparing operation results of the target circuit to perform the test of the target circuit.

Pouya teaches a configurable test access mechanism having a sliced input wrapper, output wrapper and scan configuration wrapper coupled to a circuit under test. The input wrapper efficiently adds a PRPG (pseudo-random pattern generator) function to a scan test structure without impacting speed and power requirements. The output wrapper efficiently adds a MISR (multiple input signature register) functionality for additional test purposes to implement a built-in self-test (BIST) apparatus. Use of existing scan structures to implement the PRPG and MISR functions provides significant savings of circuitry. Variability of test polynomials is easily user programmed.

Udawatta teaches an apparatus with a generator to generate a pattern and multiple scan chains configured to receive the pattern from the generator. Multiple signature registers coupled to the scan chains, to receive an output of at least one of scan chains during a mode of the integrated device.

In contrast, Applicant's independent claim 1 recites, in pertinent part:

> "A built-in self-test controller, comprising ... a pattern generator seeded with a first primitive polynomial; and a multiple input signature register capable of storing the results of an executed logic built-in self-test, the contents thereof being stored per a second primitive polynomial; wherein the first primitive polynomial has a first number of bits and the second primitive polynomial has a second number of bits, wherein the second number is different from the first number." (Emphasis added).

Independent claims 8, 12, 22 and 29 recite similar combinations of features.

Neither McNamara nor Kim, taken singly or in combination, teach or suggest this combination of features. In particular, Applicant can find no teaching or suggestion in any of the cited references of a pattern generator seeded with a first primitive polynomial and storing the results of an executed logic built-in self-test per a second primitive polynomial, wherein the first primitive polynomial and the second primitive polynomial have a different number of bits. In the Office Action, the Examiner admits that McNamara and Kim fail to teach the first and second polynomials being a certain number of bits, wherein the second polynomial has a number of bits different from the first. The Examiner also notes that Pouya suggests the polynomials be different polynomials, but does not specifically state they be different in the number of bits. However, the Examiner asserts that Pouya boasts of reduced test cost in column 1, lines 35-40, and further asserts that motivated as suggested, one with ordinary skill in the art would add the variable polynomial capabilities to the McNamara and Kim references in order to decrease test costs. Applicant submits that this suggestion by Pouya is not equivalent to a suggestion of first and second primitive polynomials having different numbers of bits, as recited in the independent claims.

With regard to the Udawatta reference, the Examiner contends that the first and second primitive polynomials having a different number of bits is taught by Udawatta at column 2, lines 17-67 and in column 3, lines 59-61. In particular, the Examiner points to column 3, lines 59-61 of Udawatta, which states: "Also, the invention can support MISRs with different polynomial sizes by the ability to add more logic and flip flops to store larger polynomials"(emphasis added). Applicant asserts that this citation from Udawatta does not teach first and second primitive polynomials having a different number of bits, as recited in the independent claims. Furthermore, Applicant asserts that this citation does not teach two different sized MISRs as suggested by the Examiner in the Office Action. Instead, Applicant submits that this citation teaches that the size of the polynomials stored by the MISRs of Udawatta are variable in accordance with the amount of logic and flip-flops present. The Examiner also cites Udawatta at column 3,

lines 16-19: "Also, one can address the issue of aliasing by increasing the length of the MISR, which has the effect of minimizing the aliasing effect" (emphasis added). Applicant submits that this citation, as the previous one, only addresses variability in size of the MISRs, but does not teach two MISRs of different sizes. Furthermore, both of these citations are silent with respect to the size of the LFSR and whether or not it would be varied correspondingly with the size of the MISRs.

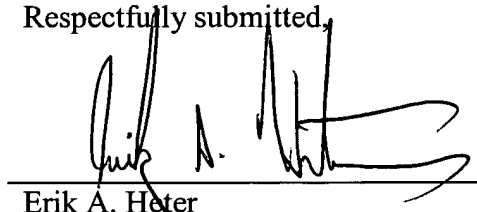
In light of these remarks, Applicant submits that Udawatta does not teach or suggest a first primitive polynomial having a first number of bits and a second primitive polynomial having a second number of bits, wherein the second number of bits is different from the first, as recited in the independent claims. Thus, Applicant submits that the cited references, taken singly or in combination, do not teach or suggest all of the elements of the independent claims and therefore a case of obviousness has not been established. With respect to the remaining rejections and the cited references, Applicant submits that the claims are not rendered obvious for at least the same reasons. Accordingly, removal of the 35 U.S.C. § 103(a) rejections is respectfully requested.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-55500/BNK.

Respectfully submitted,



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